25.6 An 84dB-SNDR Low-OSR 4th-Order Noise-Shaping SAR with an FIA-Assisted EF-CRFF Structure and Noise-Mitigated Push-Pull Buffer-in-Loop Technique

Tzuhan Wang*, Tian Xie*, Zhe Liu, Shaolan Li

Georgia Institute of Technology, Atlanta, GA

*Equally Credited Authors (ECAs)

With the combined merits of SAR and ΔΣ ADCs, the noise-shaping (NS) SAR architecture can achieve high resolution with a mild OSR, making it versatile for a wide range of applications. Nonetheless, designing a highly power-efficient NS-SAR under relatively low OSRs (<8) can be challenging. It requires the design to concurrently address two key considerations. The first is to implement high-order optimized NS with simple and low-power hardware that maximally preserves the efficient nature of the SAR. In this regard, two recent works report 4th-order NS using a cascaded EF structure [1] and an FVF-assisted CIFF structure [2] respectively, both allowing aggressive NTFs to be realized with simple open-loop amps. However, they still employ static amps/buffers, which limit the power improvement. Also, the lack of NTF optimization makes them non-ideal for low OSR designs. The second concern is the growing kT/C noise contribution under low OSR and the related large stress on the input driver. To alleviate this issue, ref [3] presents an NS-SAR with a loop-embedded input buffer that decouples the input capacitance from the kT/C noise constraint; but it suffers from a large noise penalty introduced by the buffer and the separated CDAC. Alternatively, a sampling noise cancellation (SNC) technique is proposed in [4] to facilitate a smaller CDAC value. However, owing to imperfect cancellation caused by circuit non-idealities, the CDAC can remain considerably large.

This paper presents a low-OSR 4th-order NS-SAR that effectively resolves both concerns, realizing high resolution and built-in buffering with low power. It proposes a fully dynamic EF-CRFF NS scheme empowered by an open-loop floating-inverter-amplifier (FIA)-assisted resonator. It enables a robust, optimized NTF without the cost of static-power amps, and has less trade-off compared to prior buffer-assisted integrators [2]. This work further features a buffer-in-loop technique exploiting a new sampling scheme and a push-pull source follower (PPSF) with dynamic level-shifting. It mitigates the noise-penalty and V_{CM} sensitivity, making the buffer-in-loop highly efficient and practical. The prototype in 65nm CMOS achieves 84.1dB SNDR with 500kHz BW (OSR=5) and 133.8μW (including input buffer), leading to a 180dB FoM_s. Measurement verifies that it can be driven by a signal source with an impedance as high as 2kΩ.

The signal-flow diagram of the proposed 4th-order EF-CRFF NS scheme is depicted in Fig. 25.6.1. To ensure adequate noise suppression under low OSRs, it is desirable to employ complex zeros in the NTF. Complex zeros can be generated using a resonator (i.e., two integrators in negative feedback), or an EF structure with proper FIR coefficients [5]. Typically, resonator zeros are more PVT-robust than their EF counterpart, but they need two low-loss integrators, which implies a higher circuit cost. This work combines both the EF and resonator (i.e. CRFF) approaches to balance the NS sharpness, robustness, and complexity. The two structures are arranged in the nested format [4], with the CRFF path serving as a 2nd-order sub-ADC. Such an arrangement is advantageous, as it relaxes the CRFF power consumption while keeping the EF path to only 2nd-order, which is reasonably robust. To further minimize CRFF power while realizing high-quality complex zeros, this work proposes an open-loop dynamic-amp-assisted integration method, as shown in Fig. 25.6.1. For simplicity, a single-ended version is shown. At the end of each cycle, by connecting the integration input ($V_{res}[k-1]$) with the current result ($V_{int}[k-1]$) in series, the new integrated value will be created at the amp input. The amp then transfers this new result to a temporary holding cap C_0. During the next conversion, the voltage on C_{INT} will first be erased, then loads the new result from C_0 through charge sharing. By setting the amp gain (G) and charge sharing ratio (K_1) to be reciprocal, this implements a very low-loss integrator. Note that, unlike closed-loop integrators, G need not be large and thus simple amps will suffice. In our case, the FIA is adopted. Compared to the buffer-assisted integrator [2], our scheme confers several advantages. First, it is truly dynamic, while the latter only utilizes duty-cycling, which still draws static current and needs start-up time. Second, an FIA offers lower input-referred noise than a buffer. Moreover, it does not require ping-pong caps as the latter, thus it has simpler routing. Figure 25.6.1 also shows the simulated SQNR vs. amp gain. It can be seen that the EF-CRFF scheme exhibits good robustness under gain variation.

Figure 25.6.2 illustrates the circuit schematic of the proposed NS-SAR ADC. G_1 (also an FIA), C_{EF} and FIR form the EF path, while C_{INT2-3}, C_{O2-3} and G_{2-3} form the CRFF path, with C_{O3a} serving as the resonator feedback. The signal summations of the two paths are done through cap stacking. The integrator voltages are represented in a single-sided fashion [2], so that the number of stacking caps can be reduced, which helps reduce parasitic-induced inaccuracy. The nominal gains for G_1, G_2, and G_3 are around 15, 16, and 16, respectively. As shown in the timing graph, G_2 and G_3 have a delayed firing time compared to G_1. This arrangement is to prevent the relatively large kick-back from G_1 from affecting the gain of G_2 and G_3.

To address the input driving concern, this work employs a buffer-in-loop technique, which embeds the input buffer as part of the SAR structure with relaxed linearity requirements [3,6]. However, existing buffer-in-loop implementations have several drawbacks that limit their practicality. Firstly, buffer-in-loop separates the CDAC from the sampling cap, as shown in Fig. 25.6.2. During sampling, the input is sampled onto C_S while the CDAC performs reset. The CDAC reset noise and Cs sampling noise will add up during the conversion, causing two-fold kT/C noise. Also, the buffer is in the path of the residue extraction, thus potentially adding more noise. Finally, V_{CM} mismatch between the input and DAC causes buffer non-linearity to leak out. Unlike prior designs, our buffer-in-loop scheme utilizes three strategies to overcome these drawbacks. First is a new sampling scheme. Instead of directly connecting to the buffer, we connect the input in series with the reset CDAC and the buffer during sampling. Through this, a replica of the CDAC reset noise will be captured on C_S. Since CDAC and C_S are in series during conversion, the DAC reset noise will be automatically canceled, thus avoiding the noise penalty. We also leverage the EF-reused SNC technique to suppress the C_S kT/C noise and size [4] to relax the buffer requirements.

On top of the new sampling scheme, we also improve the buffer circuit. Instead of using simple SF as in prior works, this design highlights the use of a PPSF, as shown in Fig. 25.6.3. The PPSF not only offers better g_m efficiency from current reuse, but also has unrestricted slew rate and superior linearity. This lowers the buffer's noise contribution and the V_{CM} mismatch sensitivity. In traditional amp design, biasing a PPSF can be tricky as it needs a floating level shifter. This work addresses this aspect efficiently by exploiting the CDAC switch-cap operation to provide dynamic level-shifting. We split the CDAC into two identical halves, each is fed to the PPSF NMOS or PMOS respectively. During the CDAC reset phase, the half DACs sample V_{B_HI}/V_{B_LO} from the bias gen. When the input connects in series with the CDAC during sampling, it will be naturally level-shifted at the PPSF inputs. Last but not least, the use of an FIA in this work in fact further lowers the PPSF noise impact. The self-quenching operation of the FIA shrinks the amplification BW, hence inherently suppressing the total PPSF noise, as shown in Fig. 25.6.3. Simulation verifies that the PPSF/FIA combination has much less buffer noise contribution than using PPSF with a standard G_m-R amp.

The prototyped NS-SAR is fabricated in 65nm CMOS, occupying an active area of 0.075mm^2. Operating with 5MHz Fs and a 1.1V supply voltage, the ADC consumes 133.8μW (breakdown in Fig. 25.6.4). The DAC mismatch is calibrated in the foreground. The measured output spectrum is shown in Fig. 25.6.4. It presents clear 4th-order NS, leading to an 84.1dB SNDR and 97dB SFDR with 500kHz BW (OSR = 5), respectively. The dynamic range (DR) is 84.9dB. The proposed ADC is verified to have good tolerance to input-DAC V_{CM} mismatch and source impedance, as shown in Fig. 25.6.5. The SNDR remains above 82.5dB with +/-10% V_{CM} mismatch. It can be driven by a source impedance up to 2kΩ without significant loss in SNDR. We also measured the SNDR and SFDR across temperatures and chips. It shows a robust performance with less than 1.5dB SNDR variation across test cases. Figure 25.6.6 summarizes the performance and compares it with state-of-the-art NS-SARs. Using the FIA-assisted EF-CRFF NS implementation and noise-mitigated push-pull buffer-in-loop, this work reports the first NS-SAR to achieve close to 14 ENOB under a low OSR of 5, with a high FoMs of 182.4dB and 180dB with and without buffer power, respectively. It is also the first ADC with an embedded input buffer to reach 180dB FoMs to our best knowledge. The input driver contributes less than 50% of the total power, significantly improving over prior embedded buffer designs.

References:

[1] L. Jie et al., "A 4th-Order Cascaded-Noise-Shaping SAR ADC with 88dB SNDR Over 100kHz Bandwidth," *ISSCC*, pp. 160-162, Feb. 2020.

[2] J. Liu et al., "A 250kHz-BW 93dB-SNDR 4th-Order Noise-Shaping SAR Using Capacitor Stacking and Dynamic Buffering," *ISSCC*, pp. 369-371, Feb. 2021.

[3] T. Kim and Y. Chae, "A 2MHz BW Buffer-Embedded Noise-Shaping SAR ADC Achieving 73.8dB SNDR and 87.3dB SFDR," *IEEE CICC*, pp. 1-4, Apr. 2019.

[4] T. -H. Wang et al., "A 13.8-ENOB 0.4pF-CIN 3rd-Order Noise-Shaping SAR in a Single-Amplifier EF-CIFF Structure with Fully Dynamic Hardware-Reusing kT/C Noise Cancelation," *ISSCC*, pp. 374-376, Feb. 2021.

[5] S. Li et al., "A 13-ENOB 2nd-order noise-shaping SAR ADC realizing optimized NTF zeros using an error-feedback structure," *ISSCC*, pp. 234-236, Feb. 2018.

[6] M. Krämer et al., "14b 35MS/S SAR ADC achieving 75dB SNDR and 99dB SFDR with loop-embedded input buffer in 40nm CMOS," *ISSCC*, pp. 284-285, Feb. 2015.

 978-1-6654-2800-2/22/$31.00

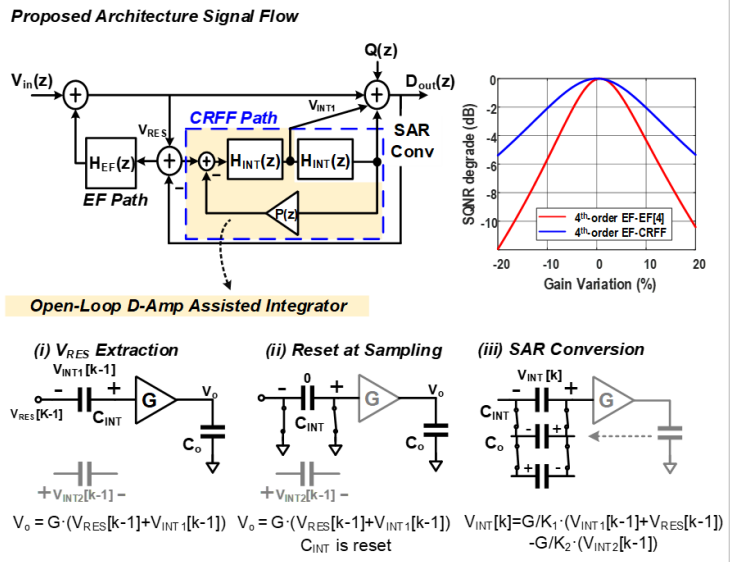

Figure 25.6.1: Signal flow of the proposed EF-CRFF architecture and D-amp-assisted integrator operation.

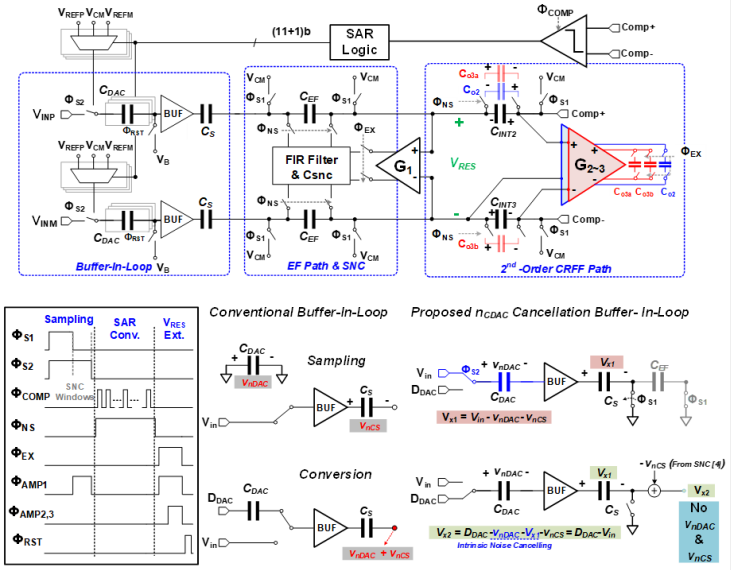

Figure 25.6.2: Circuit diagram of the proposed NS-SAR and the noise-mitigated buffer-in-loop technique.

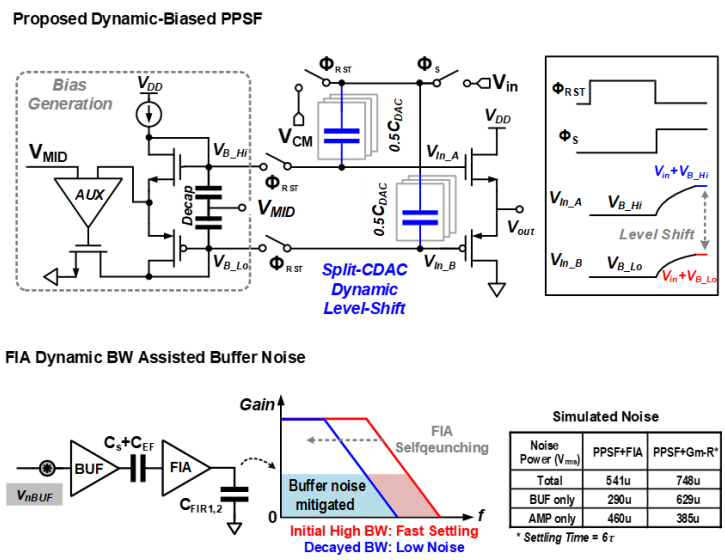

Figure 25.6.3: Proposed dynamic-biased PPSF with FIA assisted noise reduction.

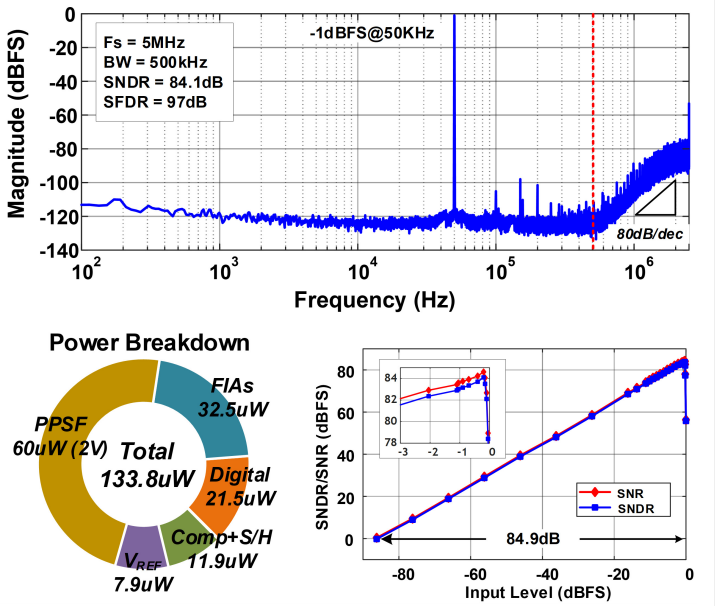

Figure 25.6.4: Measured output spectrum, power breakdown and dynamic range.

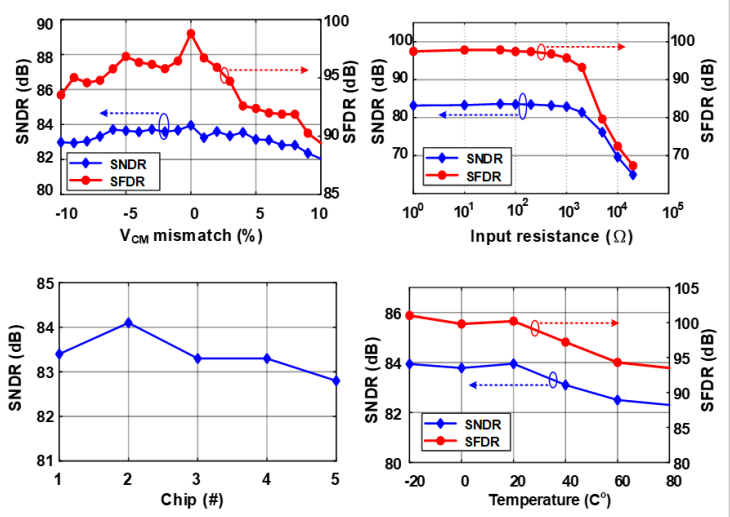

Figure 25.6.5: Measured SNDR/SFDR across V_{CM} mismatch, input resistance, chip samples and temperature variation.

	ISSCC 20 Tang	ISSCC 20 Lu	ISSCC 21 Wang	ISSCC 21 Liu	CICC 19 Kim	This Work
Process [nm]	40	28	65	40	65	65
Architecture	CIFF	EF-EF	EF-CIFF	CIFF	CIFF	EF-CRFF
NS Order	2	4	3	4	2	4
Fully Dynamic NS	✓	×	✓	×	✓	✓
kT/C Noise Suppressed	×	×	✓	×	×	✓
Input Buffered	×	×	×	×	✓	✓
Buffer Type	-	-	-	-	Source Follower	PPSF
Supply [V]	0.8/1.1	1	1.1	1.1	0.9/2.1	1.2/2
Area [mm²]	0.037	0.02	0.04	0.094	0.081	0.075
Power [uW]	107	120	119	340	870#	73.8/133.88#
Fs [MS/s]	10	2	10	5	80	5
Bandwidth [kHz]	625	100	625	250	2000	500
OSR	8	10	8	10	40	5
SNDR [dB]	83.8	87.6	84.8	93.3	73.8	84.1
DR [dB]	85.5	89	86.5	95	77	84.9
FoMs1* [dB]	181.5	176.8	182.0	182	167.4#	182.4/180.0#
FoMw** [fJ/step]	6.8	30.8	6.6	18.1	54.3#	5.6/10.2#

* FoMs1 = SNDR + 10*log10(BW/Power)
** FoMw = Power/(2^{ENOB}*2*BW)
\# With Buffer Power Included

Figure 25.6.6: Performance summary and comparison with the state-of-the-art NS-SARs.

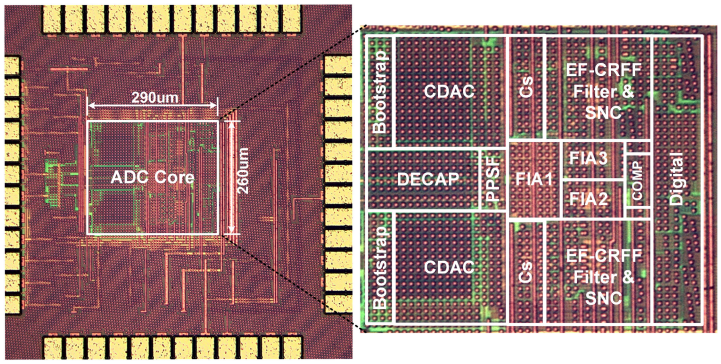

Figure 25.6.7: Die micrograph.

978-1-6654-2800-2/22/$31.00