Zhe Liu

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EDUCATION

Georgia Tech, Atlanta GA Expected May 2022

- Master of Science in Electrical Engineering GPA: 3.74/4.0

Virginia Tech, Blacksburg VA August 2016 - May 2020

- Bachelor of Science in Electrical Engineering In major GPA: 3.62/4.0 | Dean's List 6/8 semesters

CORE QUALIFICATIONS

- Hardware: Arduino, TI-MSP432, Logic Analyzers, Oscilloscopes, Power Supplies, Multimeters, Soldering.
- Computer programming languages: C, C++, Java, Python, and MATLAB.
- Circuit design and simulation: Cadence Virtuoso, HSpice, LTSpice, and basic PCB design (Altium Designer).
- Engineering modeling: Autodesk Inventor.

RELEVANT EXPERIENCES

Graduate Research Atlanta, GA

Graduate Researcher at Georgia Tech Analog Mixed Signal Microsystems and Applications (GAMMA) Lab June 2021 – Now

- Led the post-silicon measurement of a Low-OSR 4th-Order Noise-Shaping SAR ADC design. Conducted hand-soldering of SMD capacitors, resistors, LDOs, and ADC chip on PCB. Validated voltages and currents of each soldered PCB using power supply and multimeter. Presented performance measurement and compared with pre-silicon simulation results. This work has been accepted by ISSCC 2022 conference.
- Evaluated how PVT variability affects SNDR and Dynamic Range of ADC by testing multiple chips on the same PCB, tuning the voltage inputs, and controlling the temperature. Tested system robustness vs. input resistances. Recorded best SNDR of 84.1 dB, DR of 84.9 dB, and power consumption of 133.8uW. The prototyped NS-SAR ADC was fabricated in 65nm CMOS.
- Assessed the performance of different two-capacitor DAC architectures under same SAR ADC structure. Implemented transistors level circuit in Cadence and analyzed the effect of capacitance mismatch error.

6T SRAM Cell with Dynamic Power Supply Atlanta, GA

Digital System Class Project September 2021 – December 2021

- Implemented standard SRAM cell in 45-nm node with dual cell Vcc in Cadence Virtuoso for both schematic and layout. Performed statistical analysis by Monte Carlo simulation on layout netlist using Hspice. Estimated read and write failures using the method of 6σ on statistical results of Monte Carlo. Measured leakage power during idle phase on layout.
- Improved write margin from 397mV to 481mV when apply Vcc_low during write operation. Calculated read failure probability equal to 2.13% when apply Vcc_hi. Minimized write failure probability from 2.38% to 1.63%. Improved leakage power saving of 75.52%.

12-bit Pipelined SAR ADC Design Atlanta, GA

Analog System Design Class Project January 2021 – May 2021

- Designed a two-stage 12-bit differential Pipelined SAR ADC using Vcm based switching technique. Implemented the strong-arm, the NMOS/PMOS/CMOS/Bootstrap switch, and SAR logic/D flip-flop in transistors level.
- Customized two-stage clock design. Achieved sampling frequency at 31.5 MHz and ENOB of 12.68 with SNDR of 78.1519 dB. The total power consumption is 2.612 mW with FoM of 13.737 fJ/conversion-step.

Fetal Heart Sound Monitoring Device Optimization Atlanta, GA

Electrical Sub-team Leader August 2020 – December 2020

- Modified and re-designed the circuitry to improve filtering performance of a low-cost fetal heart sound monitoring device prepared for Ethiopian health care facilities.
- Achieved higher SNR by utilizing a 5th order Bessel low-pass and high-pass filter with narrow passband. Adjusted the close-loop gain. Improved the fetal heart sound detection accuracy from noisy audio signal acquired using a piezoelectric microphone.